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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Mansoori et al.	Art Unit:	2812
Serial No.:	10/620,492	Examiner:	Lindsay, Jr., W.
Filing Date:	07/16/2003	Docket No.:	TI-35375
Customer No.:	23494	Conf. No.:	9069

Title: METHOD TO REDUCE TRANSISTOR GATE TO SOURCE/DRAIN OVERLAP CAPACITANCE BY INCORPORATION OF CARBON

TRANSMITTAL OF FORMAL DRAWINGS

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Attn: Official Draftsperson

Dear Sir:

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner of Patents, P. O. Box 1450, Alexandria, VA 22313-1450.

7-28-05
Date
Marianna Smith
Marianna Smith

Submitted herewith are two replacement sheets of formal drawings.

Charge any necessary fee to Deposit Account No. 20-0668. The original and a copy of this authorization are enclosed.

Respectfully submitted,

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